

(19)



JAPANESE PATENT OFFICE

## PATENT ABSTRACTS OF JAPAN

(11) Publication number: 04028260 A

(43) Date of publication of application: 30.01.92

(51) Int. Cl

H01L 25/065  
H01L 25/07  
H01L 25/18

(21) Application number: 02133391

(71) Applicant: MATSUSHITA ELECTRIC IND CO LTD

(22) Date of filing: 23.05.90

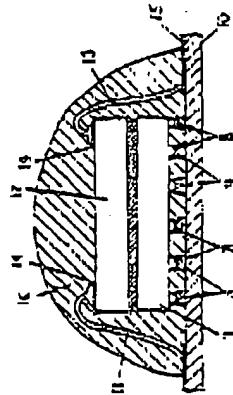
(72) Inventor: NAKANO KATSUHIRO

## (54) METHOD OF MOUNTING SEMICONDUCTOR CHIP

## (57) Abstract:

**PURPOSE:** To improve a semiconductor device in mounting density so as to miniaturize the device by a method wherein one of two semiconductor chips is mounted in a face-down manner and the other is mounted in a face-up manner, and the two semiconductor chips are mounted through a flip chip bonding and a wire bonding method respectively.

**CONSTITUTION:** Conductive bumps 8 are formed on the aluminum electrode of a first semiconductor chip 7, and the chip 7 is mounted on a board 10 in a face-down manner through the intermediary of first thermoplastic conductive resin 9. Then, a second semiconductor chip 12 is mounted on the chip 7 in a face-up manner by the use of a second thermoplastic insulating resin and can be thermally treated at a temperature lower than that of the resin 9. Furthermore, the aluminum electrodes 14 of the chip 12 are connected to wiring electrodes 15 provided to the top face of the board 10 with wires 13 through wire-bonding, and a semiconductor device is collectively sealed up with sealing material 16. By this setup, a semiconductor device can be enhanced in mounting density without increasing a board in area corresponding to the number of chips.



COPYRIGHT: (C)1992,JPO&amp;Japio